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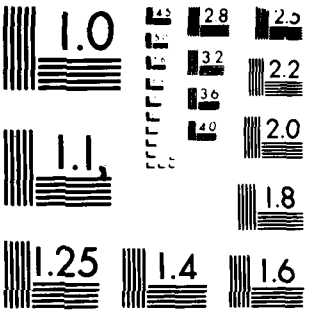

VHSIC APPLICATIONS IN EW/ESM

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ABSTRACT

The choke-point of data flow in almost every EW/ESM system is the pre-processor. Most ESM systems deal with this condition in several ways: (1) restrict sensitivity to decrease the pulse environment; (2) sample the environment either through scanning receivers, antennas, or processors. These restrictions impose a compromise on EW/ESM systems that: (1) limit the defense perimeter; (2) restrict defenses against Low Probability of Intercept (LPI) emitters; (3) limit RF band coverage; (4) restrict operation in high density signal environments. Custom and special purpose processors are expensive and often easily compromised. The most effective (cost and system) processor for EW/ESM would be a high throughput general purpose microprocessor (μP) that could be easily programmed for system needs. Analysis has shown that throughput is basically a function of memory speed matched to Arithmetic Logic Unit (ALU) speed. Memory speeds have been the principle restrictions on throughput. Special purpose and custom processors have sought to circumvent these restrictions but only at the cost of other undesirable restrictions mentioned above. With VHSIC technology, there is finally a technology that will permit the high throughput general processor required in EW/ESM. Recent experience has shown that an EW/ESM system based on general purpose processor architecture has resulted in a processor hardware/software cost of 5% of system cost. When the vendor insisted on his special purpose processor, the cost was 30% of the system. This cost went up to 50% of the system cost when the processor was custom developed for the system.

INTRODUCTION

The most severe limitation on Electronic Warfare (EW) systems is data processing. Almost every aspect of EW, ELINT, ESM, RWR, CM is choked by an ability to process data quickly enough for the sensor. These processor limitations have secondary effects upon the performance of these systems, such as operational sensitivity. In many cases, the operational sensitivity is limited to prevent system data saturation. While processor devices exist that would permit system operational improvement, weight, power, volume become incompatible with platform limitations. The DoD VHSIC (Very High Speed Integrated Circuit) program promises to provide significant improvement in Electronic Warfare, as well as most processor dependent programs in DoD [1].

An important aspect of the VHSIC program is commericial applicability. Without such long term commitment, DoD is faced with the artificial and costly support of components with only DoD need. As DoD adapted commercial hard tubes, transistors, and integrated circuits to its needs, it is important that the products of the VHSIC program have high applicability in the commercial market place. This does not relieve DoD R&D from a positive effort to stimulate VHSIC components. This stimulation should be with an eye towards long term usage such that component availability continues to support systems as near to lifetime as the rapid strides of research and development will allow. The major problem is the rapid strides of R&D such that systems must be designed to be technologically tolerant of these R&D strides for full system lifetime realization.

EW PROCESSOR REQUIREMENTS

There are a number of limitations on an EW system but invariably the most severe is the preprocessor. By way of terms of reference, an EW preprocessor is a digital subsystem that converts digital raw data (at a minimum, RF, TOA, AOA) into associated groups indicating a singular signal source. Once this grouping

has been accomplished the subsequent processing is within the hardware state-of-the-art, see Figure 1.

The data is digitized for the preprocessor and arrives on a pulse-by-pulse basis to be sorted and grouped by the preprocessor. Table 1 is a representation of the word sizes generally involved in the digitization of EW/ESM signal data. At a minimum, an EW/ESM signal must be represented by the AOA, TOA, and RF words which amount to some 41 bits of data. These raw data words are sorted and grouped in the generic preprocessor, see Figure 2. Figure 3 portrays the massive data flow that is encountered when an EW/ESM system attempts to process a high density

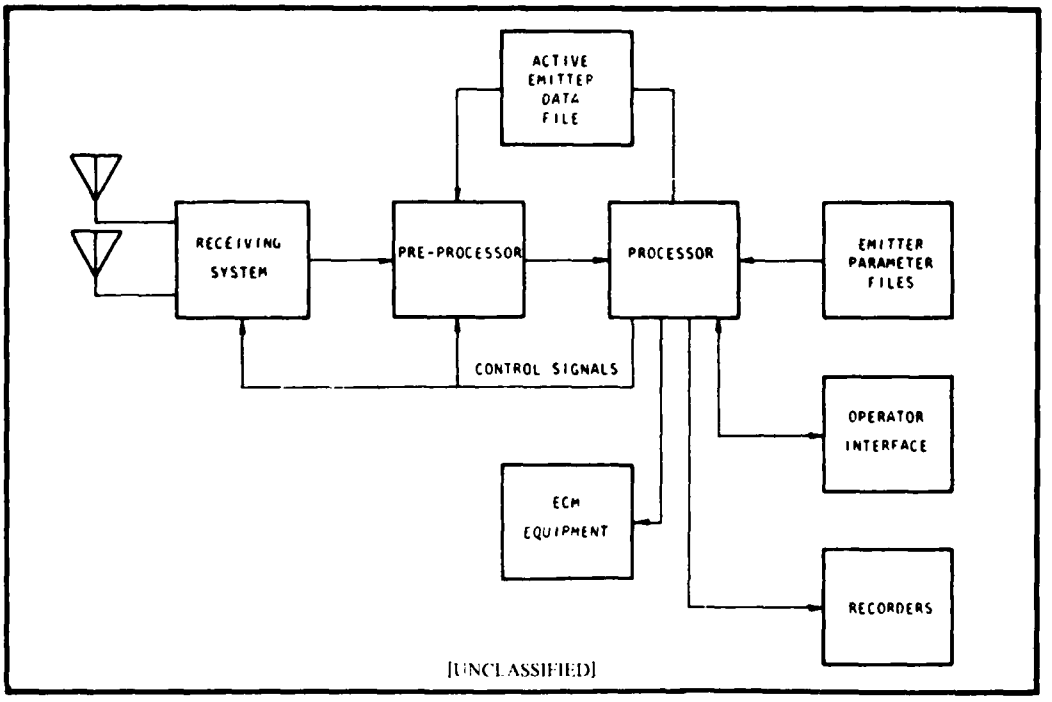

Figure 1. Generic EW/ESM system

Table 1
Representative ESM Parameters Word Size Requirements

Parameter	Range	Increments	Word Size (bits)
Angle of Arrival	0-360°	0.35°	10
Time of Arrival	0-200	0.2 μs	20
Signal Amplitude	−120 to +8 dBm	1.0 dBm	7
Pulse Width	0.25 μs		
	0-12.5 μs	0.1 μs	8
Frequency	0.5 GHz	5 MHz	
	5-10 GHz	10 MHz	11
	10-15 GHz	20 MHz	
or			
Frequency	2-4 GHZ	1 MHz	
Total			56 bits

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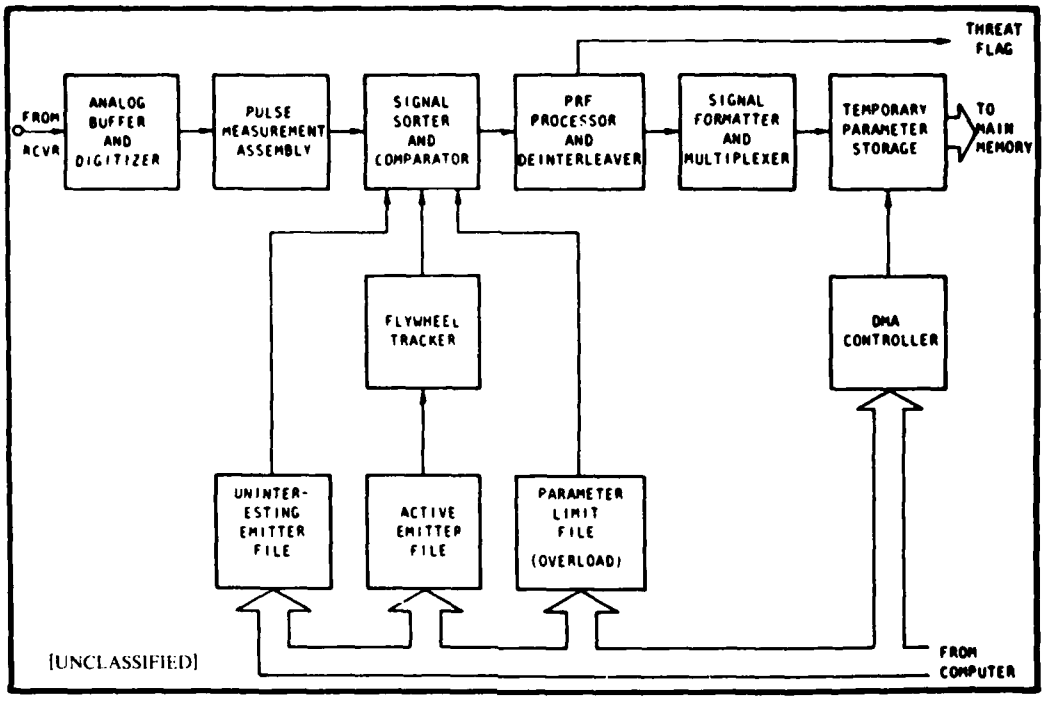

Figure 2. A generic preprocessor

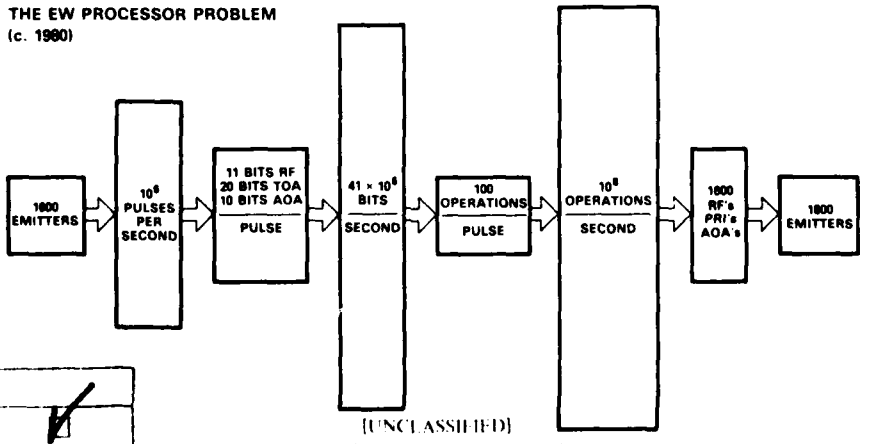

Figure 3. Preprocessor data flow

environment in real time. This figure portrays an environment of 1600 emitters that produce a million per second, see Figure 4. Each pulse is characterized by 41 bits of RF, TOA, AOA information. This generates a real time data flow of 41 million bits/seconds into the preprocessor. The preprocessor must carry out at least 100 operations on each data word (RF, TOA, AOA) in order to group the word into a cluster (identified or unidentified). This requires a preprocessor with a capacity of 300 million operations per second. Obviously, this is beyond preprocessor state-of-the-art without some compromise of the EW/ESM system. However, this exercise does portray the system limitations imposed by the preprocessor. There is, of course, a great deal of redundancy in a real time system and some of this can be eliminated with sampling.

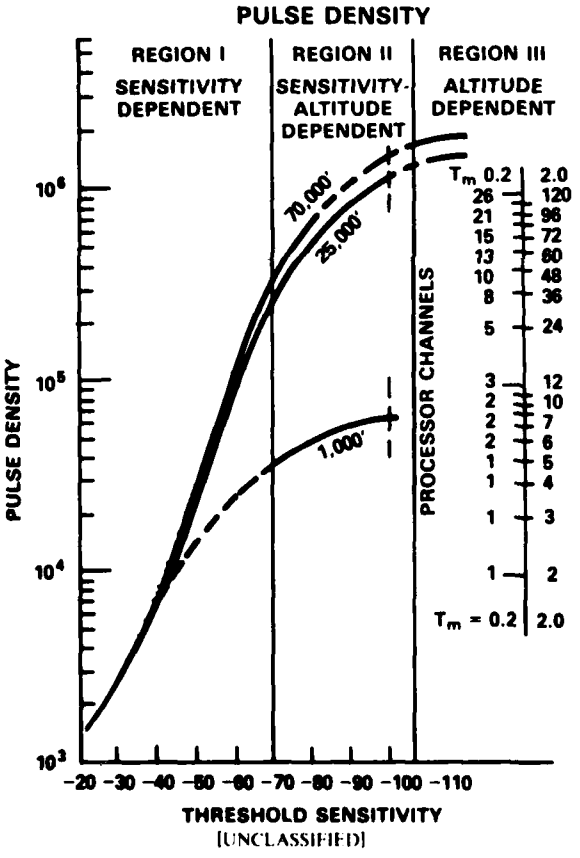

Figure 4. High density EW/ESM environment

There is a temptation to solve the problem with multiprocessor channels; however, for various reasons the multiprocessor solution is not practical. The right hand column of Figure 4 displays the number of preprocessor channels required for various pulse densities at two preprocessor technologies ($0.2 < T_M < 2.0$). With preprocessor technology of 2.0 μsec execution speed, a million pulse environment would require 120 preprocessor channels [1].

VHSIC IMPACT

The improvement of processor technology requirement is obvious from the above. However, EW/ESM requirements alone are not sufficient to drive this improvement. As a matter of fact, DoD processor requirements are not sufficient incentive to drive this improvement. Such improvement must be seen in commercial application with DoD and EW/ESM reaping the benefits along with commercial applications. It is estimated that all of DoD only represents 10% of integrated circuit demand. DoD has determined with its Tri-Service VHSIC program that it can provide some incentive to integrated circuit improvement through a well-planned , direct program of DoD needs and investment. However, such investment is primarily oriented towards commercial application from which DoD can derive a sustained source of supply.

Some confusion exists between the more commercial VLSI (Very Large scale Integrated Circuits) program and DoD's VHSIC (Very High Speed Integrated Circuits) program. VLSI is the commercial dedication to increase the number of active gates on a singular component chip. This does not in itself imply a faster processing capability. DoD's VHSIC program uses the larger (VLSI) component but stipulates a higher processing speed. The initial goals of the VHSIC program are:

Year	Lithography Resolution	Chip Density	Speed MOPS	FOM [1] Gates/sec	Equivalent [2] Technology
Present	5	12,400	0.5	5×10^{10}	
1984	1.25	75,000	1.1	$>10^{11}$	IBM 370
1986	0.5	300,000	32.0	10^{13}	20 × IBM 370's

[1] Figure-of-Merit (FOM) is the product of the number of gates on a single component and the speed that they operated

[2] On a chip

There is an ultimate limitation on the lithography resolution indicated above. Somewhere in the early 1990's technology will hit 0.25 micron resolution where the basic limitation will be the molecular granularity of the basic materials involved. It should be realized these are VHSIC goals. Some modifications are bound to be accepted depending upon the complexity of the circuits and the realization of technology limitations.

For the purposes of EW/ESM the impact of VHSIC has been projected on to current high inventory systems, Engineering Development Models (EDM's), Advanced Development Models (ADM's), and concepts. The purpose of these projections is to demonstrate VHSIC improvements that might be realized in these systems. There is no plan for such implementation since modification of the technology may not be practical. In some cases, where improvement is small, it is only because the processor impact is a small percentage of the total system. It is obvious that the greatest impact is in the airborne systems that are weight, volume, and signal density sensitive. The improvements are to the total system not just the processor subsystem.

VHSIC IMPLEMENTATION

There are a number of controversial routes in the VHSIC programs as to the architecture to pursue. One family of technologists would pursue a highly specialized circuit of limited DoD applicability, but with highly productive improvement in DoD systems. The other family would pursue a more general architecture of broad applicability with some compromise in VHSIC system improvement. The specialists argue that general architechtures will be developed without DoD incentives; whereas, specialized components will never be developed without these incentives. EW/ESM has its two camps of technologists along with DoD. The specialists would expect from VHSIC, highly special circuits that would emulate present processor functions that are accomplished with large numbers of integrated circuits. The general approach is to build a very high speed general processor that will become the programmable basis of an improved EW/ESM preprocessor.

There are a number of advantages to the general approach. The general processor is more easily replaced as technology permits improvement. The following Table 2 compares the relative characteristics of three distinct schools of processor architecture that have emerged in Navy EW/ESM. These architectures are based on actual system experience in which EW/ESM systems were implemented with general purpose processors such as the UYK-20 at a 5% of system cost. In case of the special processor architecture, the vendor insisted that his own processor be integral with the system for reasons of performance. Finally, in the case of the custom architecture, the processor is specifically designed for a specific system with no interchangeability intended. Table 2 delineates the characteristics of these three approaches. The most striking comparison is between the general purpose and custom architecture, in which for a 3-to-1 (65 vsv 22 emitters per second) improvement in performance the cost is increased 10-to-1 (50% vsv 5% of system cost).

The problems of improving the speed of a general architecture are very similar to those of a custom architecture. In the most general sense, the speed of a processor depends on matching memory speed to processor unit (ALU or CPU). In fact, the memory speed and capacity is pivotal to the processor speed [1]. The

Table 2
EW/ESM Processor Architectural Characteristics

General Purpose	Special Purpose	Custom
• Broad Familiarity	• General Military Use	• Highest Throughput
• Least Expensive	• Little Commercial Interest	• Most Expensive
• Widest Application		• Vendor Dependent
• High Commercial Use	• Requires Military Funding	• Least Versatile
• Industrially Funded		• No Commercial Interest
• Logistics Commercially Dependent	• Logistics Military Dependent	• Requires Project Funding
• 5% of System Cost	• 30% of System Cost	• 50% of System Cost
• 22 Emitters/Second	• 33 Emitters/Second	• 65 Emitters/Second

[UNCLASSIFIED]

improvement realized in custom architecture lies in accomplishing fixed circuit logic as opposed to programmable logic. The cost growth in custom architecture lies in learning. The point to be realized is that a general purpose architecture can be as technologically responsive as custom architecture and be much more cost effective.

The most current, published improvement in general purpose architecture is the work of Carver Mead at California Institute of Technology [2]. This rather complete treatment of a processor development, presents a "data path chip" architecture with the basic requirements to:

- be gracefully interconnectable for multiprocessor configuration;
- support microprogrammed control structure;
- perform variable field operations;
- be as fast as possible.

Thus, the data path chip was developed in a University atmosphere, using the latest technology to produce a high speed general processor and designated, OM (Our Machine), see Figure 5.

The OM system is composed of a number of chips, however, the unique architecture primarily lies in the Data Path Chip which after some design growth became known as OM2, see Figure 5. This chip was implemented with LSI scale circuits as class projects with various representatives of industry supplying supporting guidance, resulting in stimulating research on both sides. The resulting chips were fabricated at Hewlett-Packard's Deer Creek Laboratory, see Figures 6 and 7.

This chip was implemented using 1977-1978 technology, see Figure 8. It is a 16-bit chip with nMOS technology. Its clock period is estimated to be 135 nsec. Such a general architecture would permit the EW/ESM processing of 252 emitters per second over current general processor methods. This represents an improvement of more than an order of magnitude over the UYK-20 (22 emitters/second) for general architectures; and nearly four times improvement over current custom processing methods in EW/ESM.

The implementation of VHSIC in more custom chips for EW/ESM can be portrayed with NRL/TEWD's High Speed Signal Sorter (HSSS). HSSS is essentially a special processor to sort a dense environment by RF, AOA, and TOA. The system concentrates on the conversion of Time-of-Arrival (TOA) to Pulse-Repetition-Interval (PRI) even though it uses three parameters to sort and group, see Figure 9. The HSSS can be broken down into four hierarchial levels from which some estimation of VHSIC application and implementation can be made, see Table 3 [3].

The first column on the left are the major subsystems of the HSSS. Of these subsystems, the fastest is

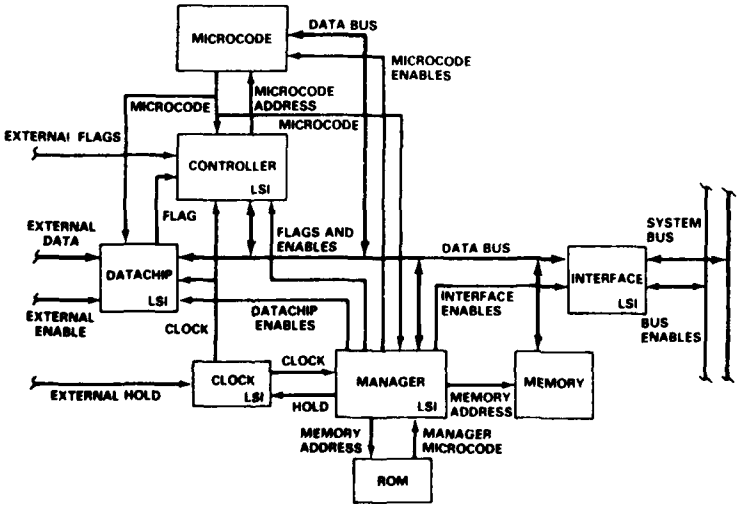

Figure 5. CALTECH's OM processor

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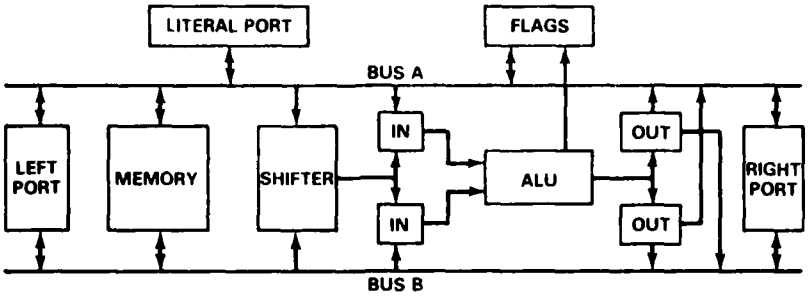

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Figure 6. OM2's block diagram

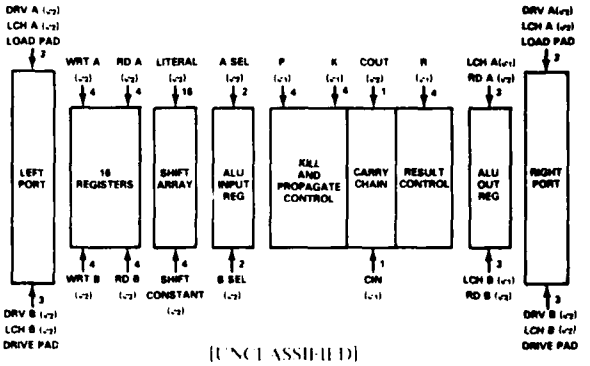

Figure 7. CALTECH's data path chip plan with wire plan

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Table 3
HSSS Hierarchy & VHSIC Requirements

LEVEL: SYSTEM	SUBSYSTEM	MODULE	CIRCUIT
• FIFO	• Emitter Characterizer	• High Speed Autocorrelator	• Tau Increment
• Parameter Gate	• Interface	• Timer	• Hex D MS/FF (8)
• TOA CAM & PGM	• Comparison	• Memory	• Dual 4-1 Mux (8)
• CPU	• Bin Manage	• Tau Increment	• 4-Bit ALU (8)
• Acquisition Processor	• Storage Bins	• TOA Compare	• Look Ahead Carry (2)
• Adaptive Tracker	• I/O Buffer	• RF	• Quad 2-Input Mux (8)
• Emitter Characterizer	• Micro-Controller	• TOA Difference	
• Buffer	• High Speed Auto Correlator	• Interface	
		• TOA/RF Processor	
VHSIC Requirements:			
Gates: 4.8×10^6	7×10^5	10^4	1012
Speed: 2 MHz	10 MHz	100 MHz	500 MHz
FOM: 9.6×10^{12}	7.0×10^{12}	1.0×10^{12}	5×10^{11}

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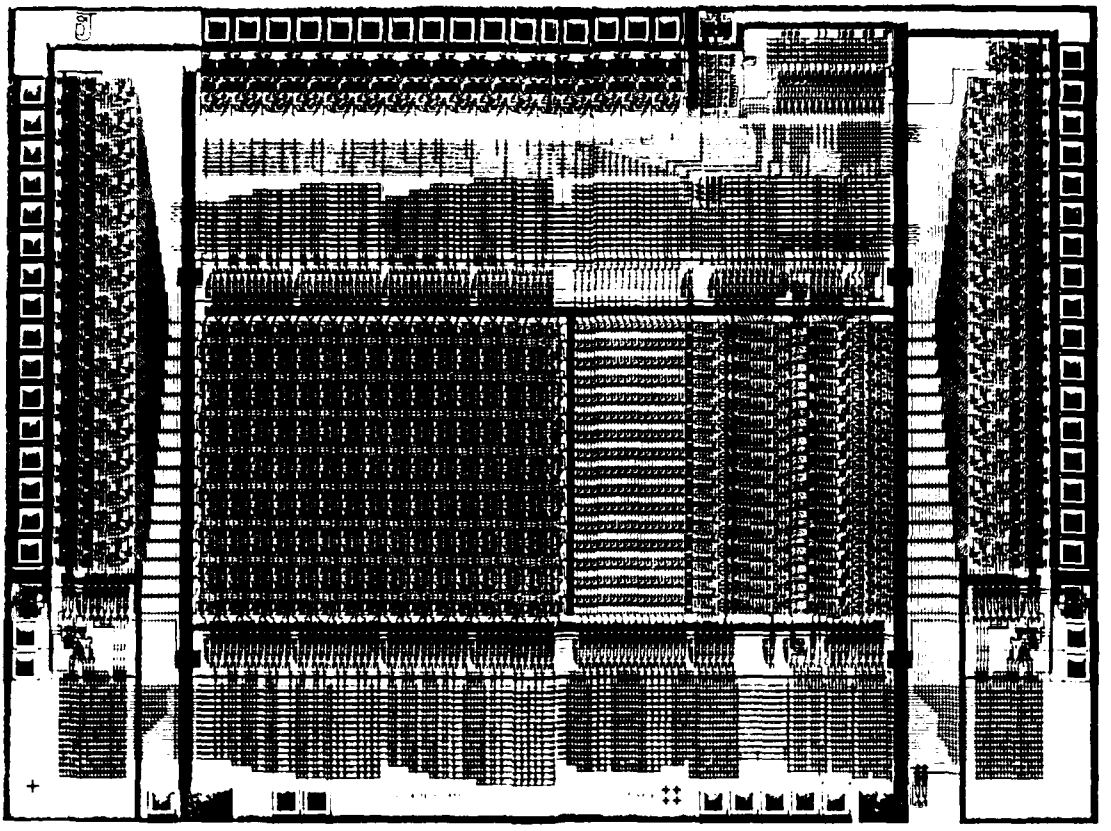

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Figure 8 CALTECH's data path chip

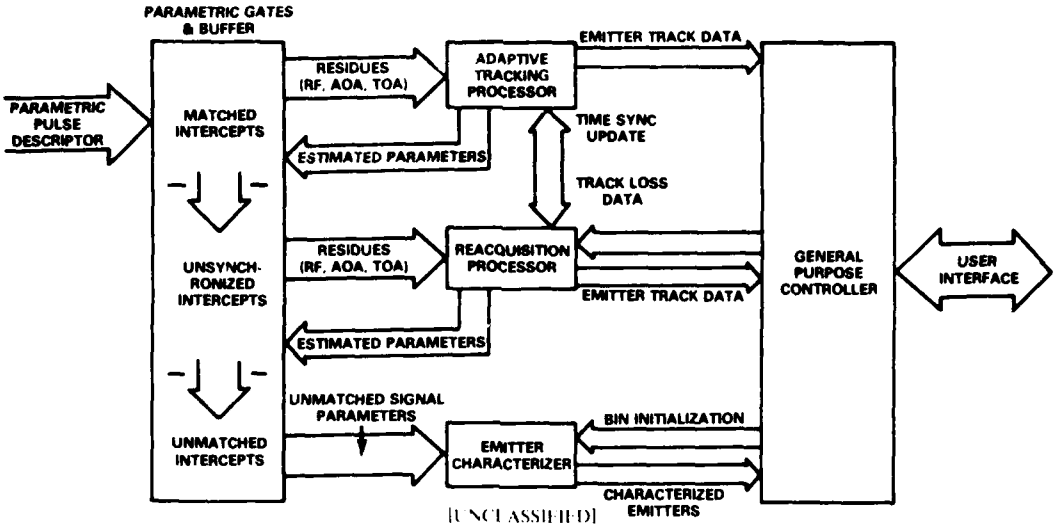

Figure 9. High speed signal sorter

the Emitter Characterizer which is highlighted and broken down into its modules in the second lefthand column under subsystems. Here again, the High Speed Autocorrelator is highlighted and broken down in the third column as the time critical module. Finally, the Tau Increment circuit of the HS autocorrelator is broken down into basic small- and medium-scale IC's. These IC's and the Tau Increment circuit were analyzed for implementation in the VHSIC program.

The final column (right hand) lists the actual IC's and their number used to make up the Tau Increment circuit. These were analyzed for the number of gates and operating speed. While the number of gates in the Tau Increment circuit is not overwhelming by VHSIC goals, the speed of operation is excessive. As a result the Figure-of-Merit (FOM) for this simplest circuit is 5 × 10^9 gates/sec. Not all of the circuits necessarily have such high critical needs (FOM's) when translated into VHSIC requirements. While not all of the circuits were analyzed, an accurate estimate of each hierarchial level was translated into VHSIC goals in the lower half of Table 3. As can be seen these goals rapidly outdistance VHSIC goals as presented earlier.

VHSIC COMMON COMPONENTS

The above discussion has concentrated on EW/ESM requirements in the VHSIC program. It has disregarded the rest of the world in usage. At this point, it would be useful to identify possible common VHSIC components that could be used in EW/ESM processors. Dominating the EW/ESM process are two functions:

- Autocorrelation
- Cross-Correlation.

Autocorrelation is principally used to convert the raw data time-of-arrival (TOA) word to pulse-repetition-interval (PRI). Cross-correlation is used to identify some set of signal characteristics (RF, AOA, PRI) with an active reference file (memory).

Dominating the implementation of the above functions are micro-instruction logic commands as opposed to arithmetic instructions which are used in other applications, see Figure 10. The reason lies in the requirement to rapidly identify a threat in a large number of emitter modes. This is simply accomplished by rapidly accessing a Random Access Memory (RAM), comparing to the current data word, and flaging a near comparison (BRANCH). Content Addressable Memories (CAM's) are attractive in concept for the above reasons; however, in implementation what they gain in rapid identification is quickly lost in speed and memory density.

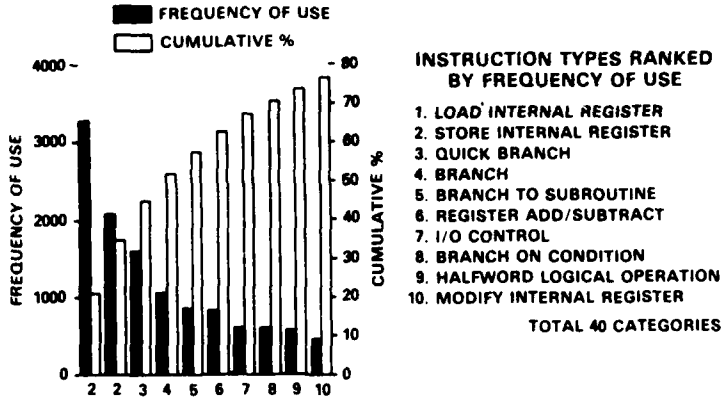

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Figure 10. Top ten microinstruction usage in EW

There are a number of VHSIC devices that would be uselul to EW/ESM, DoD, and the commercial world.

- MATRIX ADD — Compare 2048 × 32 bit words and flag comparisons within specified limits.
- AUTO-CORRELATE — On large address space, 32 bit word over 2048 × 32 bits in 10 milliseconds.
- SIGNAL TRACKER — 2048 × 64 bits words updated on average every 20 seconds.

In addition to the above, the RADAR community has identified a number of specific VHSIC configurations that would be of value to EW/ESM [4]:

- Programmable, high-speed processors which can handle floating-point operations (+< −, ×, ÷,) on complex numbers.
- Fast, high-precision analog-to-digital converters. The lack of such devices today severely restricts the application of high-speed digital technology. A suggested area of research is in the development of a floating-point A/D converter.
- Dual-port, dual-addressable high-density RAMs. All radar signal processors require moderate amounts of very-high-speed memory for variable-length delay lines and data storage.
- Programmable timers, which would count down from a basic system clock to generate the many timing pulses required to control radar operations.
- Variable-point, high-speed Fast-Fourier-transform elements, such as two-, three-, and five-point butterflies. These would be applicable in matched-filter pulse compression and doppler processing.

The Naval Material Command conducted a workshop at the Naval Air Development Center, Warminster, Pennsylvania, in which a community of signal processing representatives came together to identify their common requirements and signal processing. Their conclusions were as follows [5]:

- Hardware floating point arithmetic with eight bit exponent (minimum was overwhelmingly deemed necessary. Most sensor system designers use or expressed the desire to use parallel functional processing in their designs. True concurrency, i.e., identical or differing processing of independent, concurrent data streams, is definitely possible and desirable. This is in direct contrast to the central multiplexed arithmetic unit which, although using parallel arithmetic elements is constrained to execute a single sonar application program on

parallel data streams (channels) simultaneouly. The only exception to the desire for true functional parallelism may be in weapon processing. Electrical power and volume constraints for these systems might also constrain functional concurrency capabilities. Following from the desire for true concurrency are design features which allow a user to develop versatile parallel configurations of essentially independent elements. At the user level, such systems are transparent to the applications program and real-time executive except for system configuration of processing elements and time-line constraints.

- VHSIC chip designs, functional groups on a chip vs. "conventional" signal processor, were discussed. Questions relative to numbers of chip types, processing speeds, internal parallelism were raised. A suggested chip set was postulated for imaging radar and discussed for alternate sensor use. Macro cell functions proposed are: mulitplexer, control processor, arithmetic unit, A/D converter, RAM, and logic array.

- Two classes of environmental ranges were considered for signal processing, low, power, small size, large temperature range , and medium power, moderate size, low temperature range. Two implementation technologies might be required, thereby necessitating a dual technology architecture chip set. Minimization of off chip data transfer is highly desirable in signal processing applications.

- Present architectures have not been thoroughly tested and benchmarked using stressing signal processing application programs. Benchmark evaluations should involve evaluation programmability, i.e., ease of developing, debugging, and interpreting code. It was felt that architectures of the near term should be capable of supporting programmability out suffering significant deterioration in throughput or storage capacity reserve.

CONCLUSIONS

It should be emphasized, if not apparent from this paper, that the overall, most desirable product common to the need of most disciplines is a very high speed processor. With VHSIC goals in mind such a processor should display the characteristics of Table 4.

Table 4
General EW/ESM Processor Requirements

MICRO-INSTRUCTION	USE FREQUENCY	TIME, .t (μs)	1984 (ns)	1986 (ns)
LOAD ACCUMULATOR HALF-WORD	2073	2.289	65	2.2
MODIFY INSTRUCTION COUNTER	1598	1.398	51	1.8
STORE ACCUMULATOR HALF-WORD	1569	2.438	91	3.1
BRANCH	1043	2.129	120	4.1
BRANCH TO SUBROUTINE	834	3.371	237	8.1
LOAD INDEX REGISTER	686	1.833	200	6.9
STORE ACCUMULATOR	500	3.128	366	12.6
LOAD ACCUMULATOR	477	3.086	379	13.0
MODIFY INDEX REGISTER	464	1.622	209	7.2
SKIP IF BIT IS ZERO	447	2.914	262	13.1
I/O CONTROL	416	4.181	588	20.2
"AND" UPPER HALF-WORD	351	1.662	278	9.5
SHIFT RIGHT	349	4.114	690	23.7
SUBTRACT HALF-WORD	343	1.859	318	10.9
MODIFY STORAGE HALF-WORD	322	4.487	816	27.9
STORE INDEX REGISTER	277	2.886	610	20.9
SHIFT LEFT	267	4.400	966	33.1
ADD HALF-WORD	263	1.859	416	14.3
BRANCH ON ZERO	228	2.245	580	19.9
SKIP IF HALF-WORD IS ZERO	224	1.961	513	17.6
SKIP IF HALF-WORD IS NEGATIVE	197	2.023	606	21.0

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These characteristics are based upon an analysis of EW/ESM processor requirements (Figure 10 and Reference 1). The execution times are estimated, based upon the goals of the VHSIC program stated earlier in this paper.

Should these goals be realized the EW/ESM community can expect the technology to be available that would support system improvement as follows:

- Throughput Improvement: 22:1 By 1984, 640:1 By 1986
- System Weight Improvement: 4-6% Surface, 30% Airborne
- System Volume Improvement: 2-3% Surface, 40% Airborne
- System Cost Improvement: 6-10:1 System
- Effectiveness 40:1
- Reliability: 6:1 By 1984, 25:1 By 1986
- Number of Systems: (Navy) 850 Airborne, 340 Surface, 084 Subsurface

With the number of Naval systems alone, the improvement would be a desirable end-product.

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